

LZ95G69

Single-chip Driver LSI for CCD

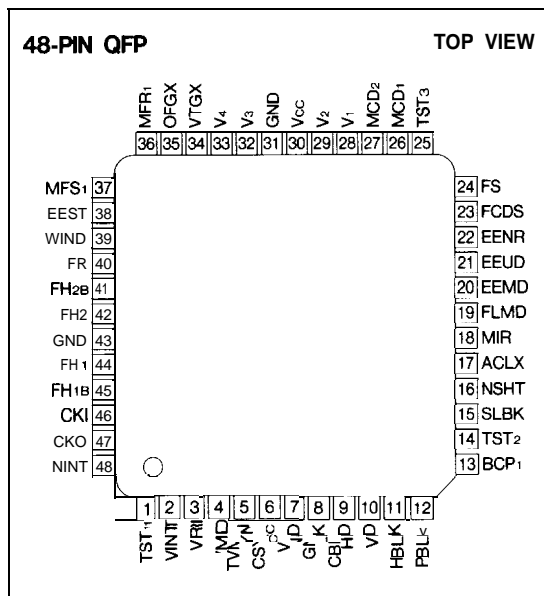
DESCRIPTION

The LZ95G69 is a CMOS single chip driver LSI which provides timing pulses used to drive a CCD area sensor, and generates synchronous pulses for TV signals and processing pulses for video signals.

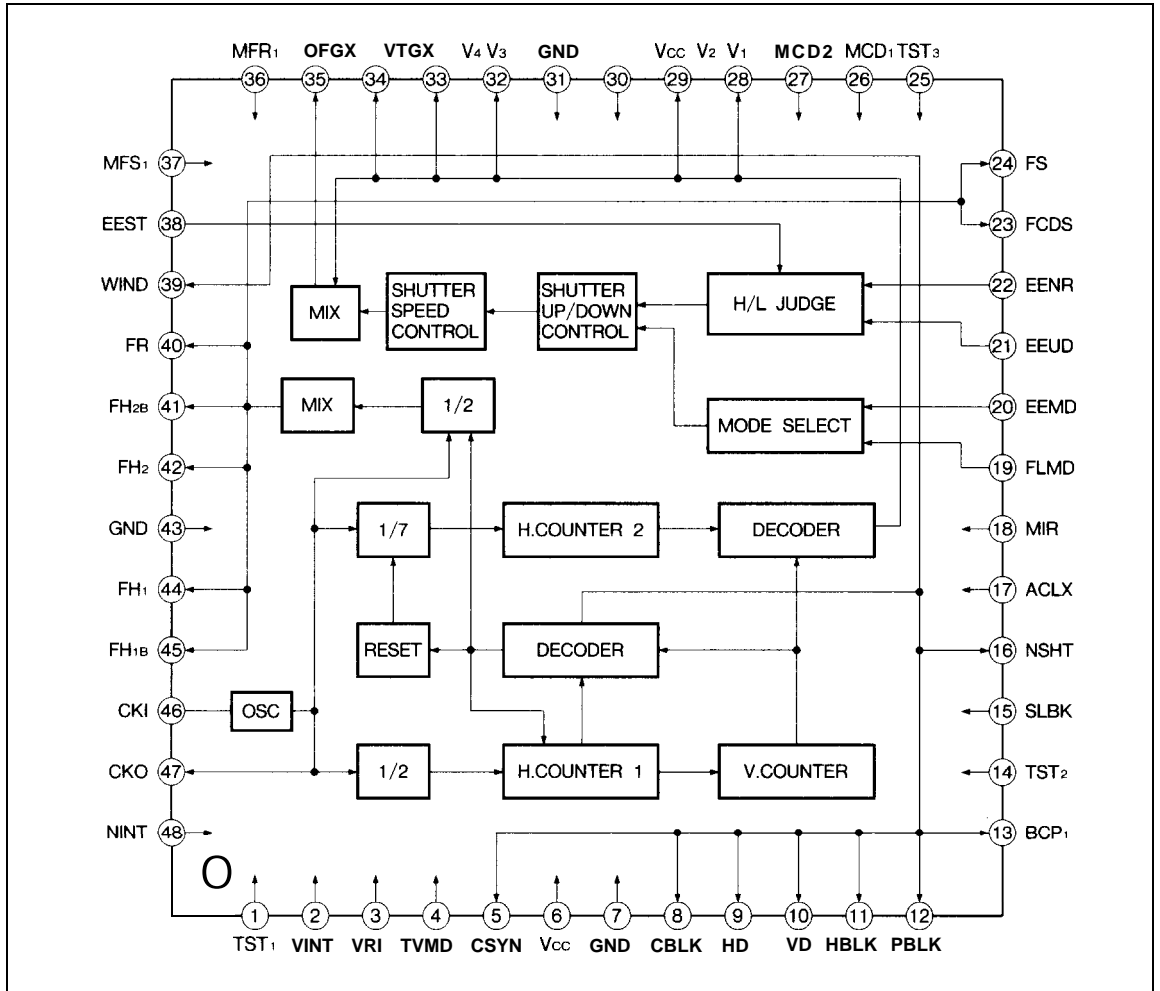
FEATURES

- Switchable between 190 000 pixels B/W CCD and 220000 pixels B/W CCD
- Switchable between EIA and CCIR systems
- Built-in EE (Electronic Exposure) control (1/60 to 1/100000 s for EIA; 1/50 to 1/100000 s for CCIR)
- Flicker-less function
- Switchable between normal and mirror image
- Non-interlace mode is possible
- External synchronization is possible
- Single +5 V power supply
- Package : 48-pin QFP(QFP048-P-101 O)

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V _{cc}	-0.3 to 7.0	v
Input voltage	V _I	-0.3 to V _{cc} + 0.3	v
Output voltage	V _o	-0.3 to V _{cc} + 0.3	v
Operating temperature	T _{opr}	-20 to +70	'c
Storage temperature	T _{stg}	-55 to +150	°C

DC CHARACTERISTICS

(V_{cc} = +5 V ± 10%, T_a = -20 to +70°C)




PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Low voltage	V _{IL}				1.5	v	1
Input High voltage	V _{IH}		3.5			v	
Input Low threshold voltage	V _{T+}				3.7	v	2
Input High threshold voltage	v _{T-}		1.0			v	
Hysteresis voltage	V _{T+} - V _{T-}		0.4			v	
Input Low current	I _{IL1}	V _I = 0 v			1.0	μA	3
	I _{IL2}	V _I = 0 v	8.0		60	μA	4
Input High current	I _{IH1}	V _I = V _{cc}			1.0	μA	5
	I _{IH2}	V _I = V _{cc}	8.0		60	μA	6
Output High voltage	V _{OH1}	I _{OH} = -2 mA	4.0			v	7
Output Low voltage	V _{OL1}	I _{OL} = 4 mA			0.4	v	
Output High voltage	V _{OH2}	I _{OH} = -6 mA	4.0			v	8
Output Low voltage	V _{OL2}	I _{OL} = 12 mA			0.4	v	
Output High voltage	V _{OH3}	I _{OH} = -9 mA	4.0			v	9
Output Low voltage	V _{OL3}	I _{OL} = 18 mA			0.4	v	


NOTES :



1. Applied to inputs (IC, ICD, ICU, IBF0).
2. Applied to input (ICSU).
3. Applied to inputs (IC, ICD, IBF0).
4. Applied to inputs (ICU, ICSU).
5. Applied to inputs (IC, ICU, ICSU, IBF0).
6. Applied to input (ICD).
7. Applied to outputs (ORI, O.SC).
(Output (oSC) measures on conditions that input (IBF0) level is 0 V or V_{cc}).
8. Applied to output (O6R12).
9. Applied to output (O6R13).

PIN FUNCTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
1	TSTI	ICD	—	Test terminal 1	A test Pin. Set open or to L level in the Normal mode.
2	VINT	ICSU	—	Initialize input	An input pin for initializing circuit. It can be used field-reset input, and the circuit is initialized with the 1/2 dividing pulse of VINT. The frequency of VINT is 60 Hz in EIA or 50 Hz in CCIR. It may be occurred jitter because of catching VINT pulse with the 1/2 dividing pulse of CKI (pin 46). The point of resetting is following, the trailing edge of VINT is advanced; At EIA mode, 0 to 148 ns from the start of ODD field, At CCIR mode, 0 to 148 ns from the start of 1st field, Set open or to H level when Internal Synchronization mode or no initializing.
3	VRI	ICSU	—	Vertical reset input /	An input pin for resetting internal vertical counter. The input pulse is necessary 1/2 horizontal max. delay from vertical synchronous start point, because VRI is counted 2 times horizontal frequency, The point of resetting is following; At EIA mode, 3.5 H from the start of VD. At CCIR mode, 3 H from the start of VD. Set open or to H level when internal synchronization or using VINT (pin 2).
4	TVMD	ICU	—	TV mode select	An input pin to select TV standards. L level : EIA mode H level or open : CCIR mode
5	CSYN	○		Composite synchronizing pulse	Composite synchronous signal output pin.
6	Vcc	—	—	Power supply	Supply +5 V power.
7	GND	—	—	Ground	A grounding pin,
8	CBLK	○		Composite blanking pulse	Composite blanking pulse. At EIA mode : H; 10.52 ns, V 20 H period. At CCIR mode : H; 11.26 ns, V 25 H period.
9	HD	○		Horizontal drive pulse	The pulse occurs at the start of lines,
10	VD	○		Vertical drive pulse	The pulse occurs at the start of every field.
11	HBLK	○		Horizontal blanking pulse	A pulse that corresponded to the cease period of the horizontal transfer pulse.
12	PBLK	○		Pre-blanking pulse	Equivalent to CBLK (pin 8) pulse except for shorter pulse width with cut-off falling edge.
13	BCPI	○		Optical black clamp pulse	A pulse to clamp the optical black signal. This pulse stays low during the absence of effective pixels within the vertical blanking.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION																						
14	TST2	ICD	-	Test terminal 2	A test pin. Set open or to L level in the Normal mode.																						
15	SLBK	ICD	-	Horizontal transfer pulse control	An input pin to control the horizontal transfer pulses [FH ₁ (pin 44), FH _{1B} (Pin 45), FH2 (Pin 42), FH _{2B} (pin 41)] L level or open : Horizontal transfer pulses is intermittently. H level : Only minimum shutter speed, horizontal transfer pulses is continually.																						
16	NSHT	○		Minimum shutter speed index	The pulse is used for detecting minimum shutter speed. When shutter speed is minimum, the pulse is High level.																						
17	ACLX	ICU	-	All clear input	An input pin for resetting all internal circuit at power on.																						
18	MIR	ICU	-	Mirror mode select	An input pin to select Mirror mode or Normal mode. L level : Normal Drive mode H level or open : Mirror Drive mode																						
19	FLMD	ICD	-	Flicker-less select	An input pin to select Flicker-less Shutter mode with EEMD (pin 20).																						
20	EEMD	ICD	-	Electronic Exposure select	An input pin to select Electronic Exposure mode with FLMD (pin 19). <table border="1"> <thead> <tr> <th rowspan="2">FLMD</th> <th rowspan="2">EEMD</th> <th colspan="2">Shutter speed (s)</th> </tr> <tr> <th>EIA</th> <th>CCIR</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>1/60</td> <td>1/50</td> </tr> <tr> <td>H</td> <td>L</td> <td>1/100</td> <td>1/120</td> </tr> <tr> <td>L</td> <td>H</td> <td>1/90 220 max.</td> <td>1/54 220 max.</td> </tr> <tr> <td>H</td> <td>H</td> <td>1/96 540 max.</td> <td>1/98 540 max.</td> </tr> </tbody> </table>	FLMD	EEMD	Shutter speed (s)		EIA	CCIR	L	L	1/60	1/50	H	L	1/100	1/120	L	H	1/90 220 max.	1/54 220 max.	H	H	1/96 540 max.	1/98 540 max.
FLMD	EEMD	Shutter speed (s)																									
		EIA	CCIR																								
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L	H	1/90 220 max.	1/54 220 max.																								
H	H	1/96 540 max.	1/98 540 max.																								
21	EEUD	IC	-	Electronic Exposure control 1	An input pin to control Electronic Exposure with EENR (pin 22).																						
22	EENR	IC	-	Electronic Exposure control 2	An input pin to control Electronic Exposure with EEUD (pin 21). <table border="1"> <thead> <tr> <th>EEUD</th> <th>EENR</th> <th>Shutter speed control</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>L</td> <td>up</td> </tr> <tr> <td>H</td> <td>H</td> <td>stop</td> </tr> <tr> <td>L</td> <td>H</td> <td>down</td> </tr> </tbody> </table>	EEUD	EENR	Shutter speed control	H	L	up	H	H	stop	L	H	down										
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23	FCDS	○		CDS pulse 1	A pulse to clamp the feed-through level from CCD.																						
24	FS	○		CDS pulse 2	A pulse to sample-hold the signal from CCD.																						
25	TST ₃	ICD	-	Test terminal 3	A test pin. Set open or to L level in the Normal mode.																						
26	MCD ₁	ICU	-	FCDS phase control input	Pins to control the phase between the FH ₁ (pin 44) and FCDS (pin 23).																						
27	MCD ₂	ICU	-																								

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
28	V ₁	0		Vertical transfer pulse 1	A vertical transfer pulse for CCD. Connect to ϕ_{V1} pin of CCD.
29	V ₂	0		Vertical transfer pulse 2	A vertical transfer pulse for CCD. Connect to ϕ_{V2} pin of CCD.
30	V _{CC}		—	Power supply	Supply +5 V power.
31	GND		—	Ground	A grounding pin
32	V ₃	0		Vertical transfer pulse 3	A vertical transfer pulse for CCD. Connect to ϕ_{V3} pin of CCD.
33	V ₄	0		Vertical transfer pulse 4	A vertical transfer pulse for CCD. Connect to ϕ_{V4} pin of CCD.
34	VTGX	0		Read out pulse	A pulse that transfers the charge of the photodiode to the vertical shift register. Connect to VTG pin of CCD through the invert and level shift circuit.
35	OFGX	0		OFG pulse output	A pulse that sweeps the charge of the photodiode for electrical shutter. Connect to OFG of CCD through the invert, level shift and DC offset circuit. It is held L at H level in Normal mode.
36	MFRI	ICU	—	FR phase control input	Pins to control the phase between FH ₁ (pin 44) and FR (pin 40).
37	MFS ₁	ICU	—	FS phase control input	Pins to control the phase between FH ₁ (pin 44) and FS (pin 24).
38	EEST	ICU	—	Electronic Exposure control 3	An input pin to control Electronic Exposure, with using EEUD (pin 21) and EENR (pin 22). L level : Electronic Exposure is stopped, H level or open : Electronic Exposure is operated.
39	WIND	0		Window pulse	A pulse for window pulse. When connected to EEST (pin 36), the operation of Electronic Exposure can be stopped at the upper side of monitor.
40	FR	0		Reset pulse	A reset pulse for CCD. Connect to ϕ_R of CCD through the DC offset circuit,
41	FH _{2B}	0		Horizontal transfer pulse 2B	A horizontal transfer pulse for CCD. Connect to ϕ_{H2B} of CCD.
42	FH ₂	0		Horizontal transfer pulse 2	A horizontal transfer pulse for CCD. Connect to ϕ_{H2} of CCD.
43	GND	—	—	Ground	A grounding pin
44	FH ₁	0		Horizontal transfer pulse 1	A horizontal transfer pulse for CCD. Connect to ϕ_{H1} of CCD.
45	FH _{1B}	0		Horizontal transfer pulse 1 B	A horizontal transfer pulse for CCD. Connect to ϕ_{H1B} of CCD.

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	FUNCTION
46	CKI	IBFO		Clock input	An input pin for reference clock oscillation. The frequencies are as follows : At EIA mode : 13.500 MHz (858 fH) At CCIR mode : 13.500 MHz (864 fH) (fH = Horizontal frequency)
47	CKO	Osc		Clock output	An output pin for reference clock oscillation. The output is the inverse CKI (pin 46).
48	NINT	Icu	—	Non-interlace select	An input pin to select Non-interlace mode. L level : Interlace mode H level or open : Non-interlace mode At Non-interlace mode, the field is ODD field and 262 H period at EIA mode, and 1st field and 312 H period at CCIR mode.

IC Input pin (CMOS level).

Icu Input pin (CMOS level with pull-up resistor).

ICD Input pin (CMOS level with pull-down resistor).

Icsu Schmitt-trigger input pin (CMOS level with pull-up resistor).

ORI Output pin.

06RI 2 Output pin.

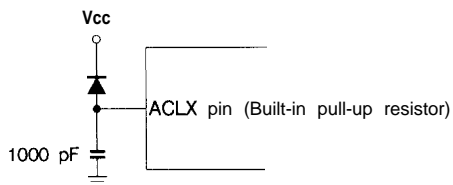
06R13 Output pin.

IBFO : Input pin for oscillation.

Osc : Output pin for oscillation.

NOTE :

1. How to use ACLX pin (pin 17)



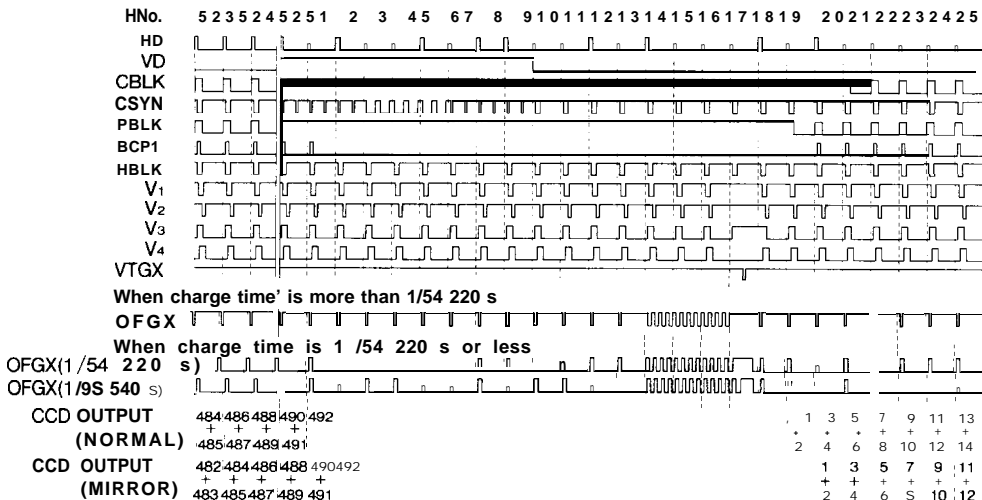
2. Shutter speed changes at Electronic Exposure Control mode

E I A		C C I R	
EXPOSURE TIME (#a)	SHUTTER SPEED (a)	EXPOSURE TIME (μs)	SHUTTER SPEED (a)
10.15	1/98540	10.15	1/98540
18.44	1/54 220	18.44	1/54 220
32.96	1/30 340	33.41	1/29 930
49.04	1/203W	49.46	1/20 210
65.11	1/15 360	65.10	1/15360
82.0	1/12203	82.4	1/12130
96.5	1/10 270	97.4	1/10 270
112.6	1/8680	113.5	1/8810
126.7	1/7 770	129.6	1/7 720
145.6	1/6 870	146.4	1/6630
160.1	1/6 250	161.4	1/6 200
176.1	1/5680	177.5	1/5 630
192.2	1/5 200	193.6	1/5170
209.1	1/4 760	210.4	1/4 750
271.6	1/3 680	273.4	1/3 660
(every 63.6 μs)		(every 64.0 μs)	
1288.5	1/776	1425.4	1/702
(every 254.2 μs)		(every 256.0 μs)	
4339.2	1/230	4625.4	1/216
(every 572.0 μs)		(every 576.0 μs)	
16351.2	1/61.1	19473.4	1/51.4

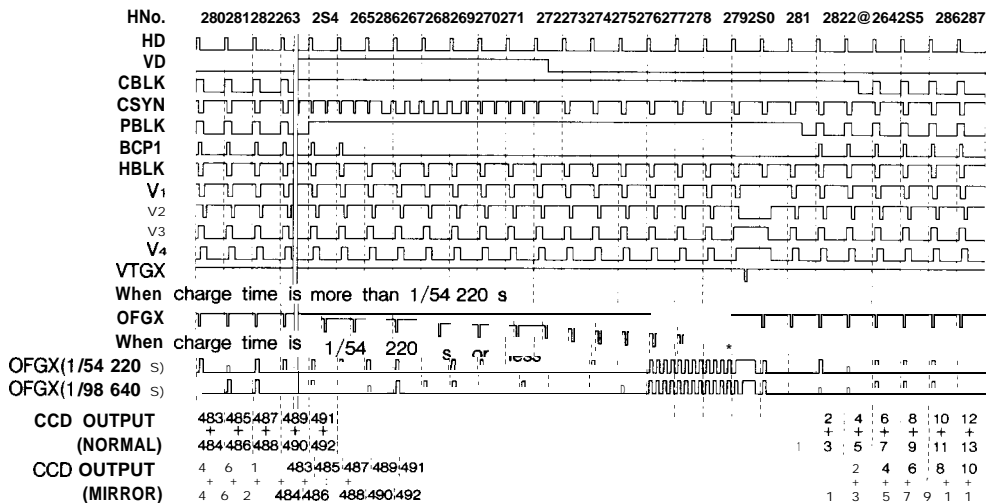
TIMING DIAGRAM

VERTICAL PULSE TIMING < NTSC >

(ODD FIELD)

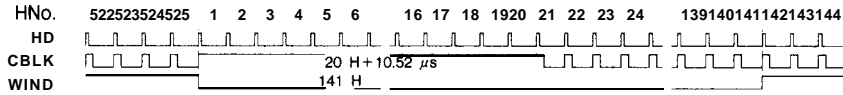


(EVEN FIELD)

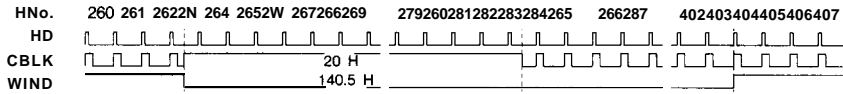


“WIND” PULSE TIMING < NTSC >

(ODD FIELD)

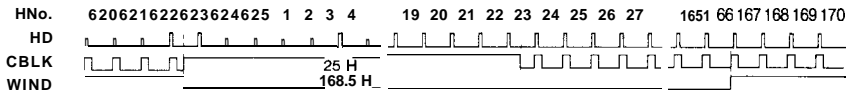


(EVEN FIELD)

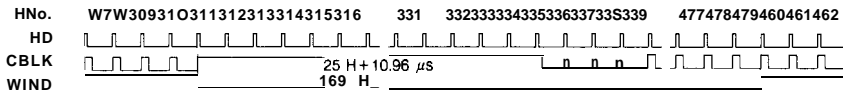


“WIND” PULSE TIMING < PAL >

(1st, 3rd FIELD)



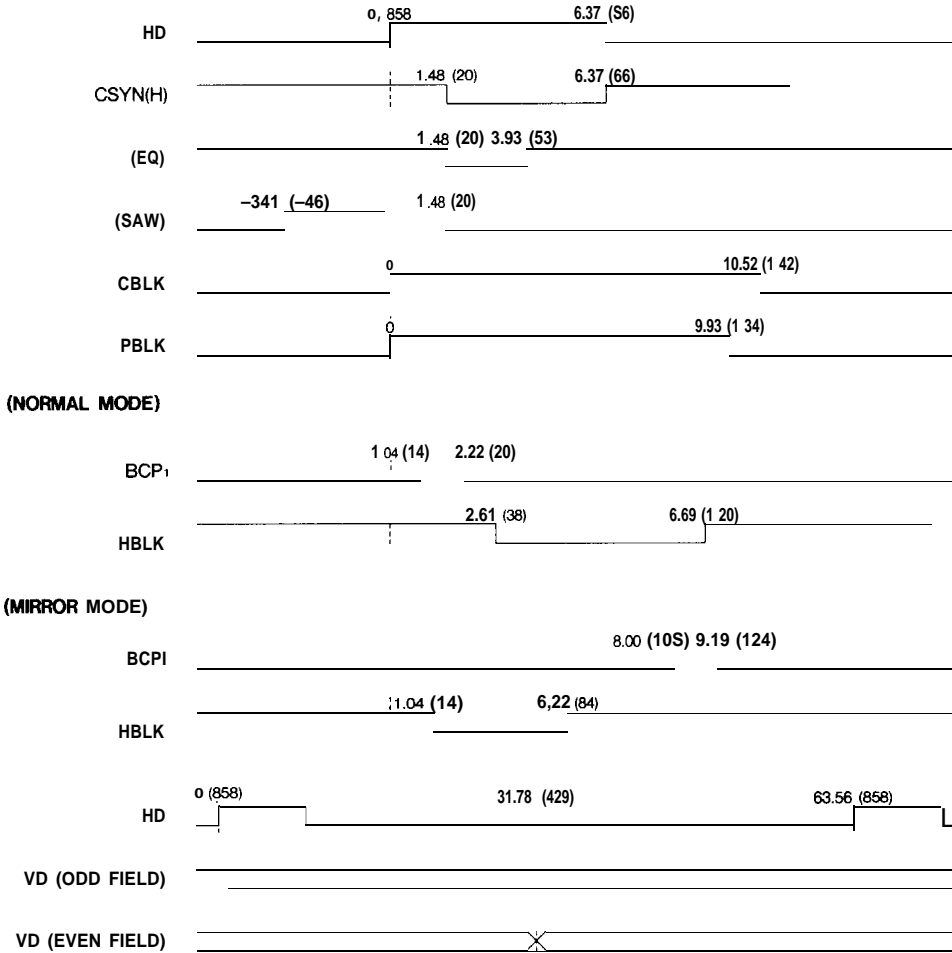
(2st, 4rd FIELD)



HORIZONTAL PULSE TIMING < NTSC >

Unit : μ S

The inside of () is a number of CKI clock.

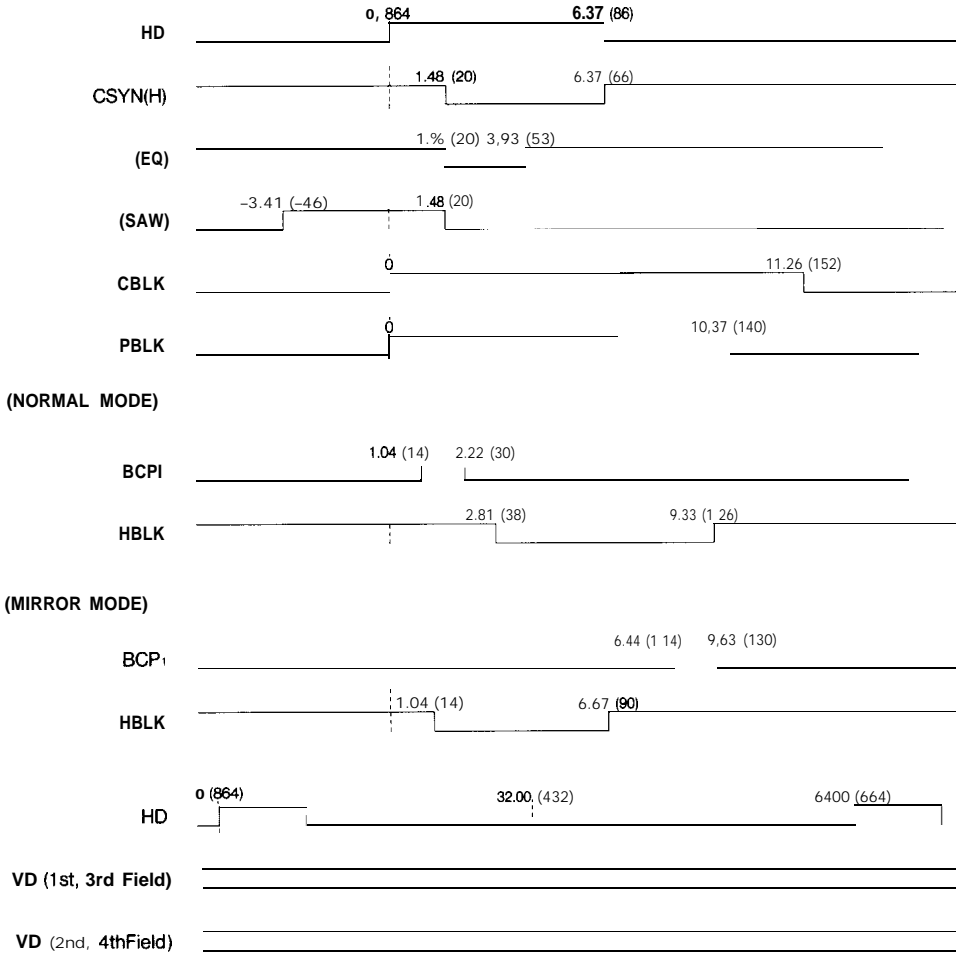


CCD PERIPHERALS
3

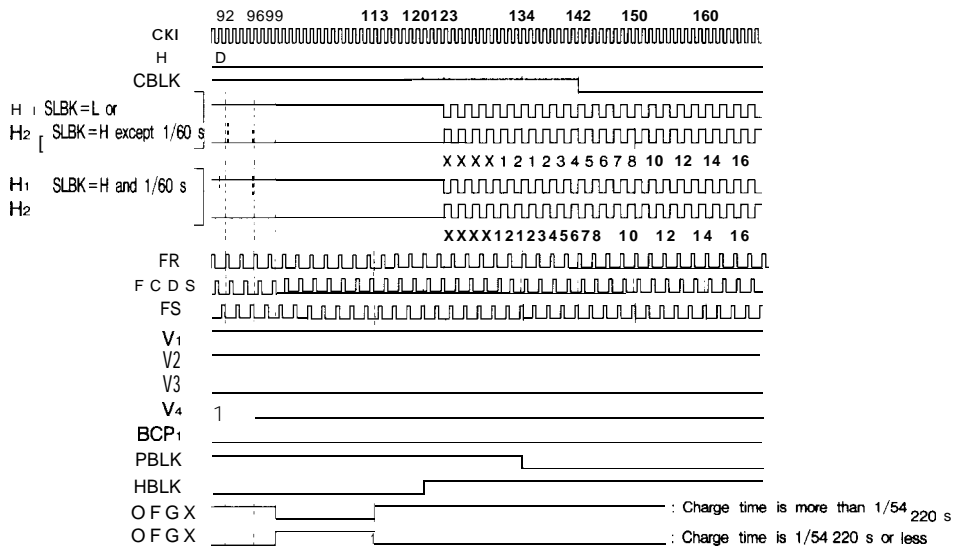
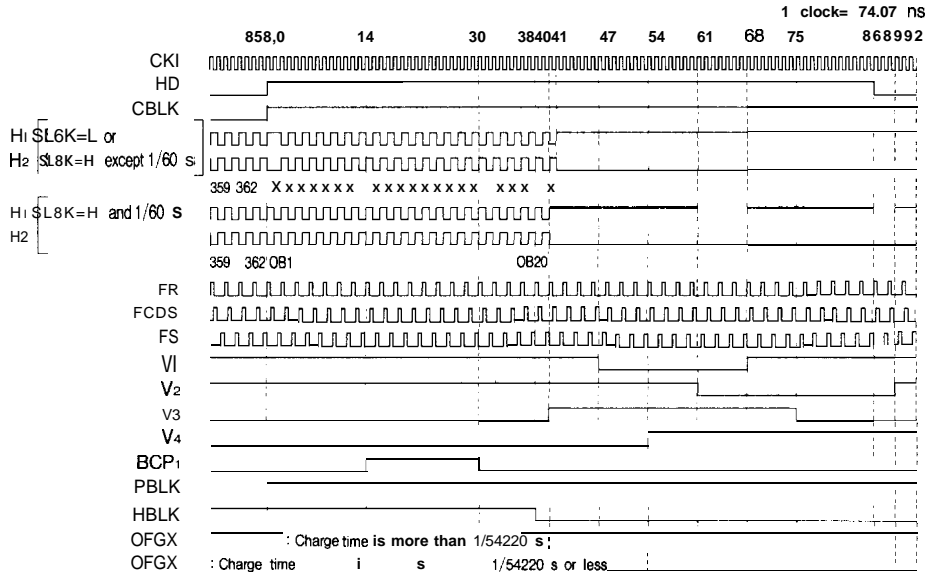
HORIZONTAL PULSE TIMING < PAL >

Unit : μ S

The inside of () is a number of CKI clock.



HORIZONTAL TIMING < NTSC, NORMAL MODE >

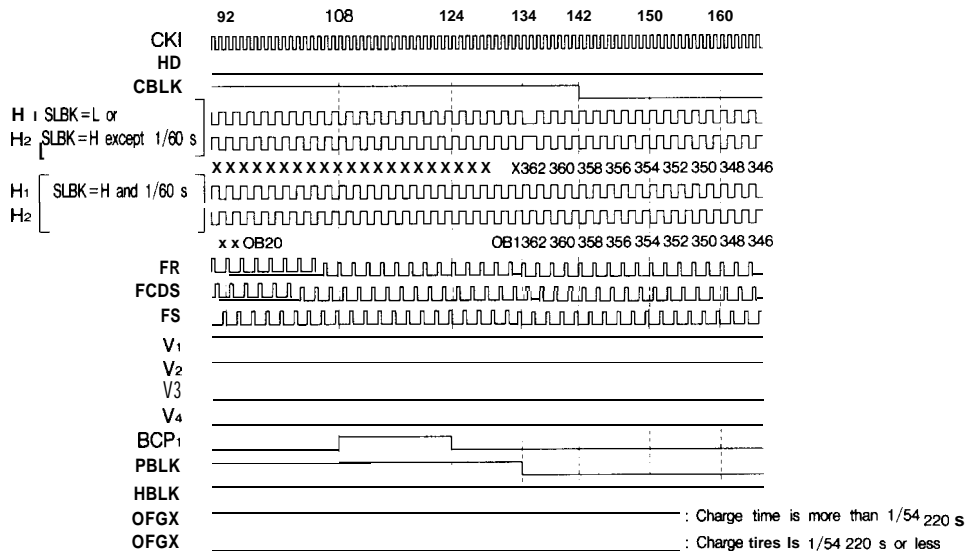
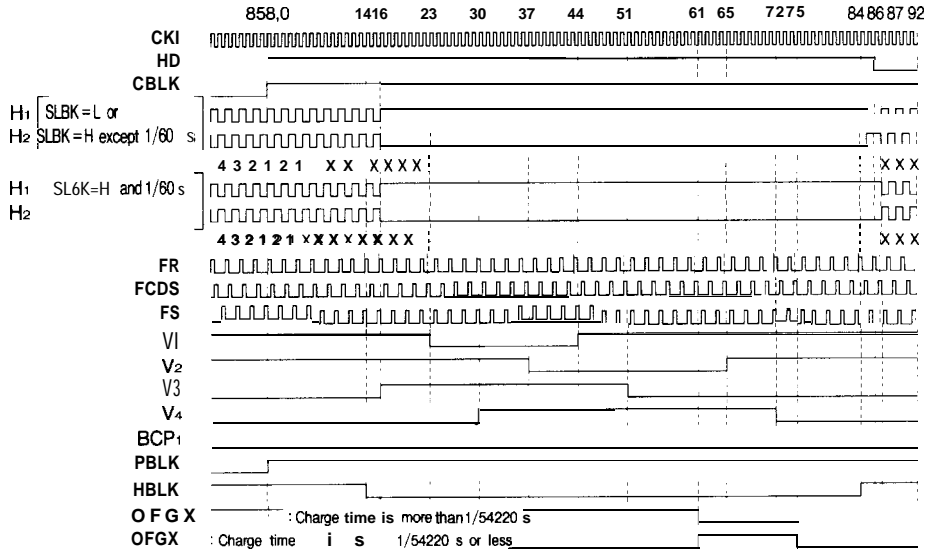


CCD PERIPHERALS



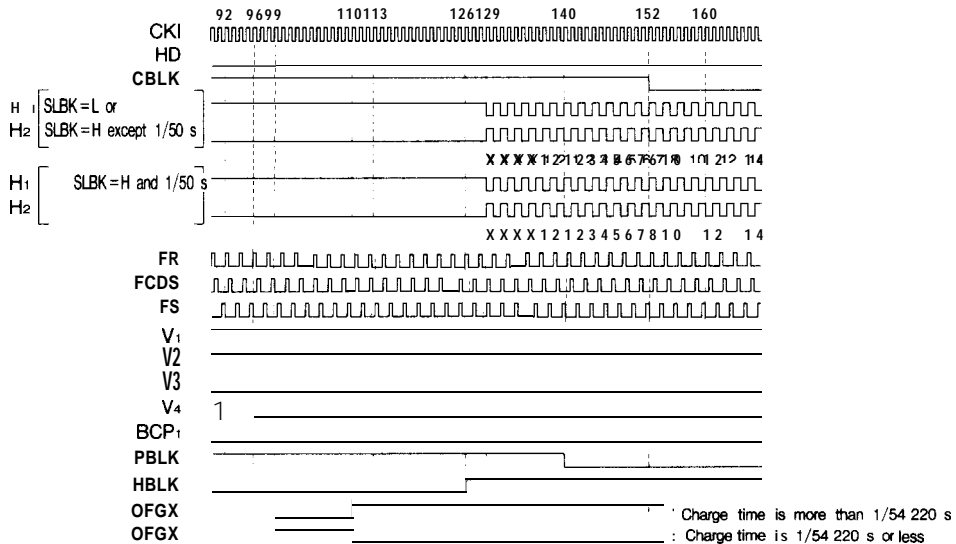
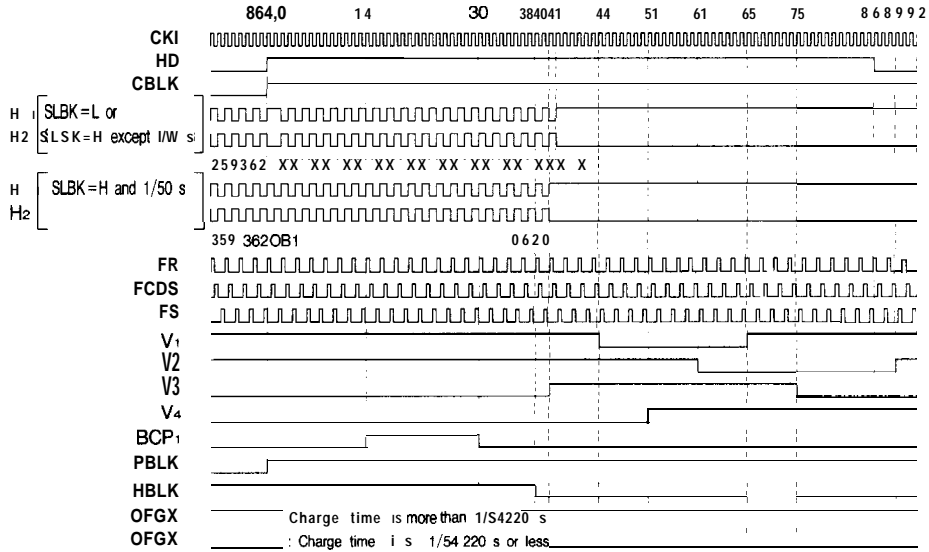
HORIZONTAL TIMING < NTSC, MIRROR MODE >

1 clock= 74.07 ns



HORIZONTAL TIMING < PAL, NORMAL MODE >

1 clock= 74.07 ns

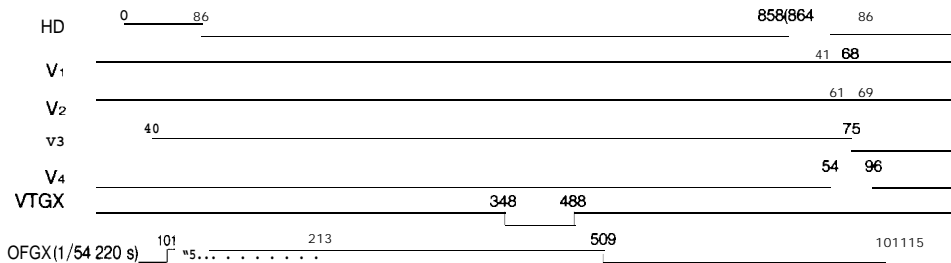


CCD PERIPHERALS

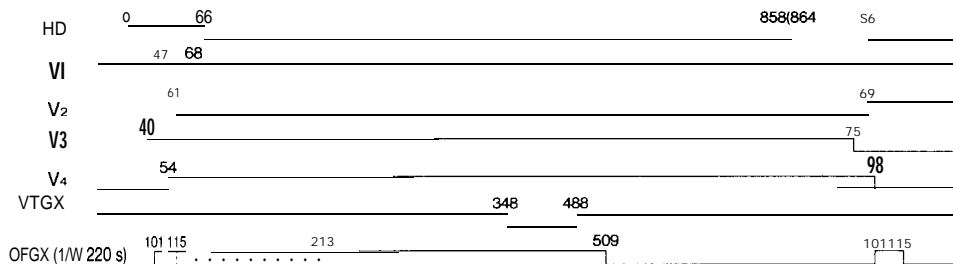


READ OUT PULSE TIMING < NORMAL MODE >

(ODD (1st, 3rd) FIELD)

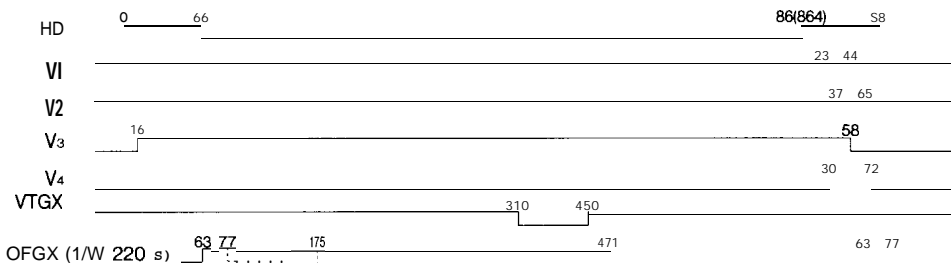


(EVEN (2nd, 4th) FIELD)

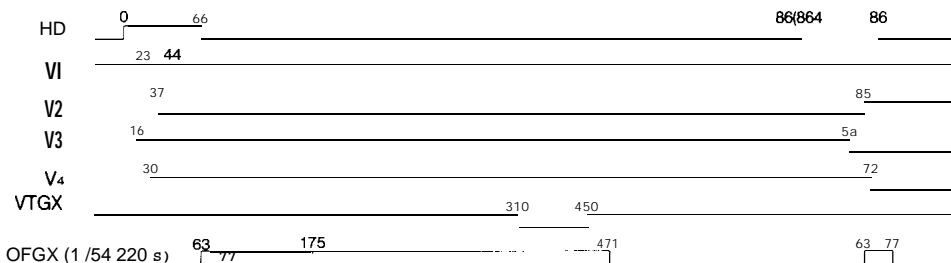


READ OUT PULSE TIMING < MIRROR MODE >

(ODD (1st, 3rd) FIELD)



(EVEN (2nd, 4th) FIELD)



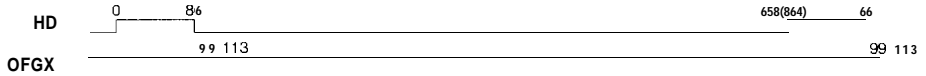
3 CCD PERIPHERALS

OFD PULSE TIMING

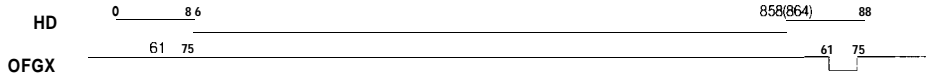
The number : clock pulse, () : PAL

• Charge time is more than 1/4780 s (1/4750 s)
 [While shutter speed changes every 9 H, 4 H, 1 H.]

(NORMAL MODE)

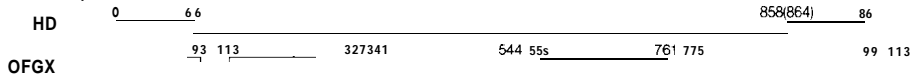


(MIRROR MODE)



• Charge time is more than 1/4780 s (1 /4750 s) to 1/54 220 s
 [While shutter speed changes every 1/4 H.]

(NORMAL MODE)



(MIRROR MODE)

